**Introduction to Computer Organisation and Architecture**

**Tutorial 9**

1. What are the types of system buses? Give examples for each type.
2. List the design issues that need to be considered in a bus.
3. Describe the following:
   1. Data bus width
   2. Address bus width.
4. If a bus has address line that could address 8Gbyte of memory, how many address lines are there?
5. If an address bus has a width of 32 lines, how many bytes of memory can it address?
6. Compare and contrast asynchronous bus and synchronous bus.
7. What are the two types of bus in terms of carrying address and data? List the attributes of each bus.
8. Describe the steps how bus arbitration is executed for the following methods:
   * Static arbitration
   * Dynamic arbitration
9. For a set-associative cache, a main memory address is viewed as consisting of three fields. List and define the three fields.

Tag, set , word

1. A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.

4k = 2^2 x 2^10

Total words = 2^2 x 2^10 x 2^7 = 2^19

Tag (8) set(4) word(7) = 19

64=2^6  
divide into 4 line set = 2^6/2^2 = 2^4

1. A two-way set-associative cache has lines of 16 bytes and a total size of 8 Kbytes. The 64-Mbyte main memory is byte addressable. Show the format of main memory addresses.

64mb = 2^6 x 2^20 = 2^26

8kb = 2^3 x 2^10 = 2^13

Line of 16 bytes = 2^13/ 2^4 = 2^9

Since is it’s 2 way so 2^9/2^1 = 2^8

Tag (14) set(8) word (4) = 26

1. Consider a machine with a byte addressable main memory of 216 bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.
2. How is a 16-bit memory address divided into tag, line number, and byte number?

Tag(8) line(5) words(3)

2^16/2^3 = 2^13 8bytes =2^3

1. Into what line would bytes with each of the following addresses be stored?

0001 0001 0001 1011 slot 3

1100 0011 0011 0100 slot 6

1101 0000 0001 1101 slot 3

1010 1010 1010 1010 slot 21

1. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?

Least signicificant bit 0001 to 1111

1. How many total bytes of memory can be stored in the cache?

256

1. Why the tag is also stored in the cache?

2 memory address can be stored in the same cache line. Tag is used to distinguish them

1. Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size.
2. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

2^32,2^26,2^6, 20 bits

Tag (26) word (6)

1. Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

2^26, no lines 26bits

1. Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in set, number of sets in cache, number of lines in cache, size of tag.

2^26 4 lines, 2^17, 2^9